



# ORIENT

## Photo coupler

### Product Data Sheet

Part Number: OR-155E

Customer: \_\_\_\_\_

Date: \_\_\_\_\_

**SHENZHEN ORIENT COMPONENTS CO., LTD**

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**1. Features**

- (1) 1.0 A maximum peak output current
- (2) 0.8 A minimum peak output current
- (3) Rail-to-rail output voltage
- (4) 200 ns maximum propagation delay
- (5) 100 ns maximum propagation delay difference
- (6) 35 kV/us minimum Common Mode Rejection (CMR) at  $V_{CM} = 1500\text{ V}$
- (7)  $I_{CC} = 3.0\text{ mA}$  maximum supply current
- (8) Wide operating range: 10 to 30 Volts ( $V_{CC}$ )
- (9) Guaranteed performance over temperature  $-40^{\circ}\text{C} \sim +105^{\circ}\text{C}$ .
- (10) Safety approval
  - UL approved(No.E323844)
  - VDE approved(No.40029733)
  - CQC approved (No.CQC22001345200 )
- (11) In compliance with RoHS, REACH standard
- (12) MSL Level 1



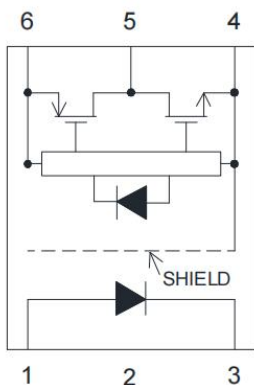
**2. Description**

The OR-155E optocoupler is ideally suited for driving power IGBTs and MOSFETs used in motor control inverter applications and inverters in power supply system. It contains an AlGaAs LED optically coupled to an integrated circuit with a power output stage. The 1.0A peak output current is capable of directly driving most IGBTs with ratings up to 1200V/50A. For IGBTs with higher ratings, the OR-155E series can be used to drive a discrete power stage which drives the IGBT gate. The Optocoupler operational parameters are guaranteed over the temperature range from  $-40^{\circ}\text{C} \sim +105^{\circ}\text{C}$ .

**3. Application Range**

- (1) Plasma Display Panels (PDPs)
- (2) Plasma Display Panel
- (3) IGBT/MOSFET gate drive
- (4) Uninterruptible power supply (UPS)
- (5) Industrial Inverter
- (6) Induction heating

**4. Functional Diagram**



Truth Table			
LED	High side	Low side	VO
OFF	OFF	ON	Low
ON	ON	OFF	High

- 1: Anode
- 3: Cathode
- 4: GND
- 5:  $V_O$ (Output)
- 6:  $V_{CC}$

Note: A 0.1- $\mu\text{F}$  bypass capacitor must be connected between pin 6 and pin 4

## 5. Absolute Maximum Ratings (Ta=25°C)

Parameter		Symbol	Rated Value	Unit
Input	Average Forward Input Current	$I_F$	25	mA
	Peak transient input forward current	$I_{FPT}$	1	A
	Reverse Input Voltage	$V_R$	5	V
	Input power dissipation	$P_D$	40	mW
Output	“High” Peak Output Current	$I_{OH(PEAK)}$	1.0	A
	“Low” Peak Output Current	$I_{OL(PEAK)}$	1.0	A
	Output Collector Power Dissipation	$P_O$	250	mW
Input Current (Rise/Fall Time)		$t_{r(IN)} / t_{f(IN)}$	500	ns
Supply Voltage		$V_{CC}$	35	V
Output Voltage		$V_O$	35	V
Insulation Voltage		$V_{iso}$	3750	V <sub>rms</sub>
Output IC Junction Temperature		$T_J$	125	°C
Working Temperature		$T_{opr}$	-40 ~ + 105	°C
Storage Temperature		$T_{stg}$	-55 ~ + 125	
*2 Soldering Temperature		$T_{sol}$	260	

\*1. Room temperature = 25 °C. Exceeding the maximum absolute rating can permanently damage the device. Working long hours at the maximum absolute rating can affect reliability.

\*2. soldering time is 10 seconds.

## 6. Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
Operating Temperature	$T_A$	-30	105	°C
Supplier Voltage	$V_{CC}$	10	30	V
Input Current (ON)	$I_{F(ON)}$	7	16	mA
Input Voltage (OFF)	$V_{F(OFF)}$	-3.0	0.8	V

**7. Electrical Optical Characteristics at Ta=25°C**

	Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input	Input Forward Voltage	$V_F$	1.2	1.4	1.8	V	$I_F = 10\text{mA}$
	Input Forward Voltage Temperature Coefficient	$\Delta V_F / \Delta T$	—	-1.25	—	mV/°C	$I_F = 10\text{mA}$
	Input Reverse Voltage	$BV_R$	5	—	—	V	$I_R = 10\mu\text{A}$
	Input Threshold Current (Low to High)	$I_{FLH}$	—	2.0	5	mA	$V_O > 5\text{V}, I_O = 0\text{A}$
	Input Threshold Voltage (High to Low)	$V_{FHL}$	0.8	—	—	V	$V_O < 5\text{V}, I_O = 0\text{A}$
	Input Capacitance	$C_{IN}$	—	35	—	pF	$f = 1\text{MHz}, V_F = 0\text{V}$
Output	High Level Supply Current	$I_{CCH}$	—	2.0	3.0	mA	Output Open, $I_F = 7\text{ to }16\text{mA}$
	Low Level Supply Current	$I_{CCL}$	—	2.0	3.0	mA	Output Open, $V_F = -3\text{ to }+0.8\text{V}$
	High level output current	$I_{OH}$	—	—	-0.3	A	$V_O = (V_{CC} - 1.5\text{V})$
			—	—	-0.8		$V_O = (V_{CC} - 3\text{V})$
	Low level output current	$I_{OL}$	0.3	—	—	A	$V_O = (V_{EE} + 1.5\text{V})$
			0.8	—	—		$V_O = (V_{EE} + 3\text{V})$
	High level output voltage	$V_{OH}$	$V_{CC} - 0.6$	$V_{CC} - 0.35$	—	V	$I_F = 10\text{mA}, I_O = -100\text{mA}$
	Low level output voltage	$V_{OL}$	—	$V_{EE} + 0.25$	$V_{EE} + 0.4$	V	$I_F = 0\text{mA}, I_O = 100\text{mA}$
	UVLO Threshold	$V_{UVLO+}$	—	8.0	—	V	$V_O > 5\text{V}, I_F = 10\text{mA}$
		$V_{UVLO-}$	—	6.5	—	V	$V_O < 5\text{V}, I_F = 10\text{mA}$
UVLO Hysteresis	$UVLO_{HYS}$	—	1.0	—	V		

Note 1. All Typical values at  $T_A = 25^\circ\text{C}$  and  $V_{CC} - V_{EE} = 30\text{V}$ , unless otherwise specified;

Note 2. Maximum pulse width = 50  $\mu\text{s}$ .

Note 3. Maximum pulse width = 10  $\mu\text{s}$ .

## 8. Switching Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Propagation Delay Time to High Output Level	$t_{PHL}$	50	115	200	ns	$R_g = 47\Omega$ , $C_g = 3nF$ , $f = 10\text{ kHz}$ , Duty Cycle = 50% $I_F = 7\text{ to }16\text{ mA}$ , $V_{CC} = 15\text{ to }30\text{ V}$ $V_{EE} = \text{ground}$
Propagation Delay Time to Low Output Level	$t_{PLH}$	50	115	200		
Pulse Width Distortion	PWD	—	15	70		
Propagation delay difference between any two parts or channels	PDD	100	—	100		
Output Rise Time (20 to 80%)	$T_r$	—	35	—		
Output Fall Time (80 to 20%)	$T_f$	—	35	—		
Common mode transient immunity at high level output	$ CM_H $	35	50	—	kV/ $\mu\text{s}$	$T_A = 25^\circ\text{C}$ , $I_F = 10\text{ to }16\text{ mA}$ , $V_{CM} = 1500\text{ V}$ , $V_{CC} = 30\text{ V}$
Common mode transient immunity at low level output	$ CM_L $	35	50	—	kV/ $\mu\text{s}$	$T_A = 25^\circ\text{C}$ , $V_F = 0\text{ V}$ , $V_{CM} = 1500\text{ V}$ , $V_{CC} = 30\text{ V}$

Note 1. All Typical values at  $T_A = 25^\circ\text{C}$  and  $V_{CC} - V_{EE} = 30\text{ V}$ , unless otherwise specified;

Note 2:  $CM_H$  is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic high state ( $V_O > 15\text{ V}$ ).

Note 3:  $CM_L$  is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic low state ( $V_O < 1\text{ V}$ ).

Note 4: The difference between  $t_{PHL}$  and  $t_{PLH}$  between any two parts series parts under same test conditions.



## 9. Order Information

### Part Number

# OR-155E-W-Y-Z

### Note

155E = Part number.

W = Tape and reel option. (TP or TP1).

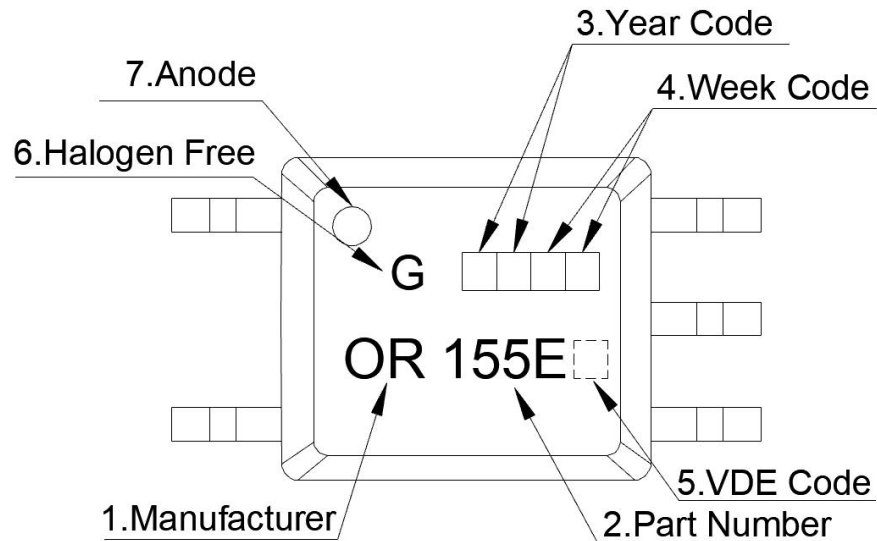
Y = 'V' code for VDE safety (This options is not necessary).

Z = 'G' code for Halogen free.

\* VDE Code can be selected.

Option	Description	Packing quantity
S(TP)	Surface mount lead form (low profile) + TP tape & reel option	3000 units per reel
S(TP1)	Surface mount lead form (low profile) + TP1 tape & reel option	3000 units per reel

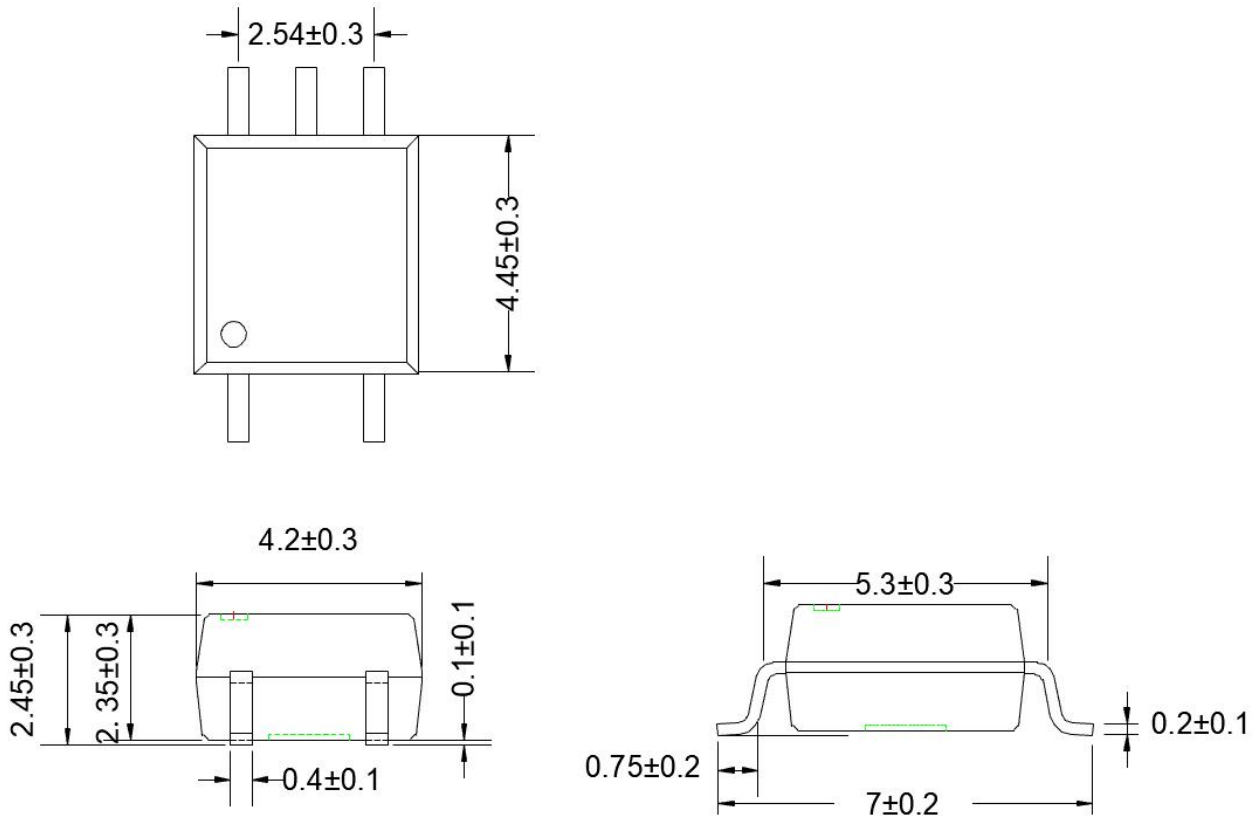
## 10. Naming Rule



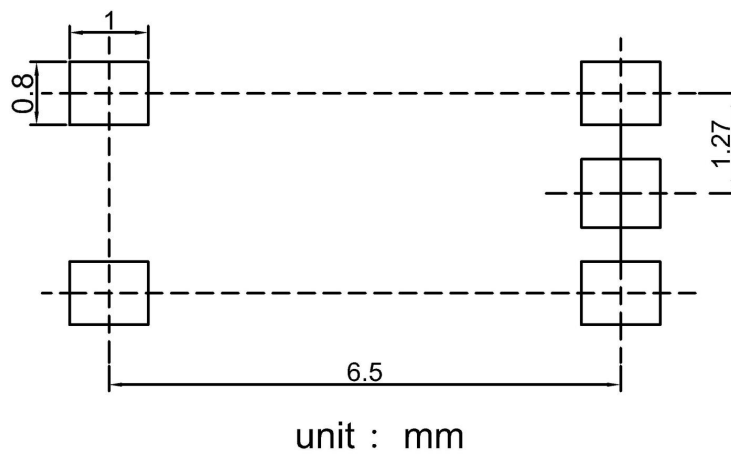
1. Manufacturer : ORIENT.
2. Part Number : 155E.
3. Year Code  : '21' means '2021' and so on.
4. Week Code : 01 means the first week, 02 means the second week and so on.
5. VDE Code . (Optional)
6. Halogen free code.
7. Anode.

\* VDE Mark can be selected.

### 1. Outer Dimension



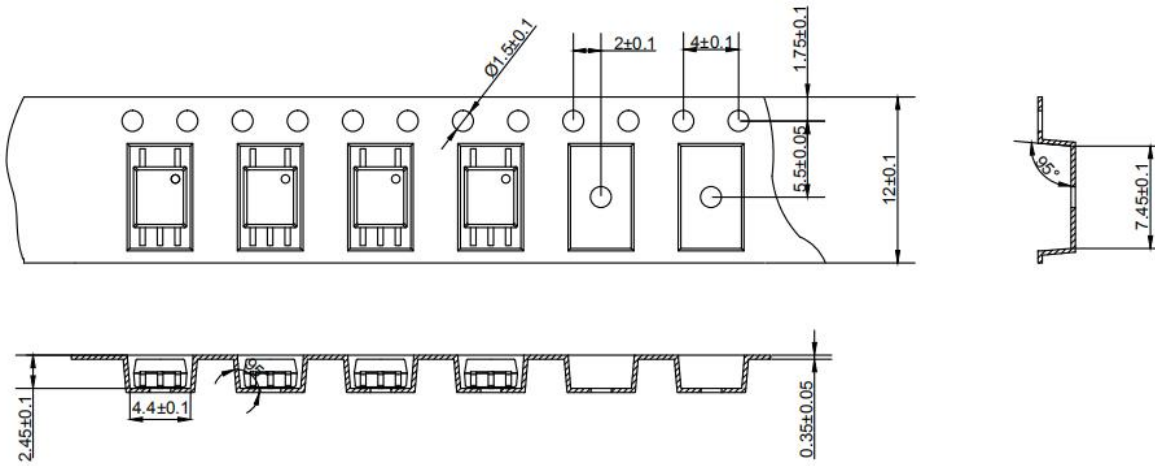
### 2. Recommended Foot Print Patterns (Mount Pad)



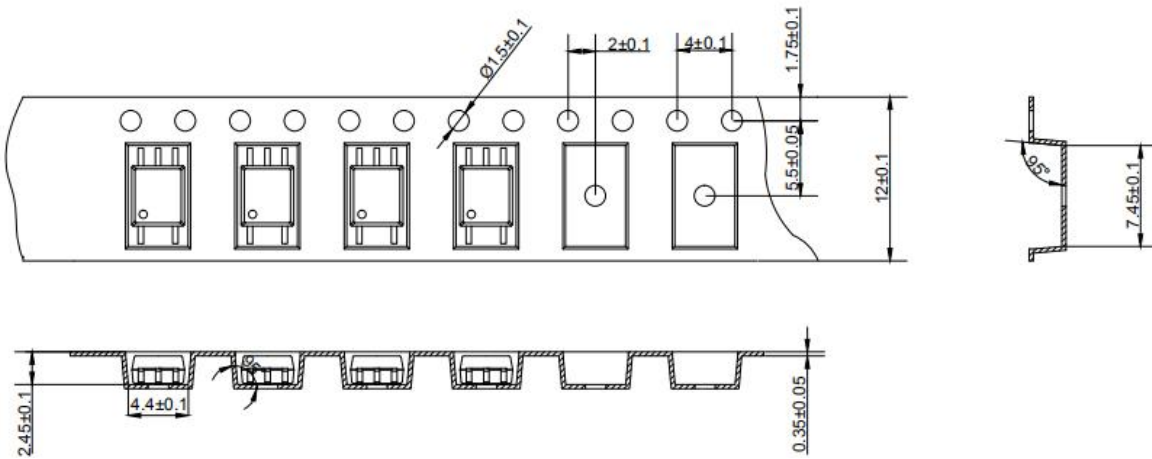


### 3. Taping Dimensions

#### (1) OR-155E-TP



#### (2) OR-155E-TP1



Description	Symbol	Dimension in mm(inch)
Tape wide	W	$12 \pm 0.3$ (0.472)
Pitch of sprocket holes	P0	$4 \pm 0.1$ (0.157)
Distance of compartment	F	$5.5 \pm 0.1$ (0.217)
	P2	$2 \pm 0.1$ (0.079)
Distance of compartment to compartment	P1	$8 \pm 0.1$ (0.315)

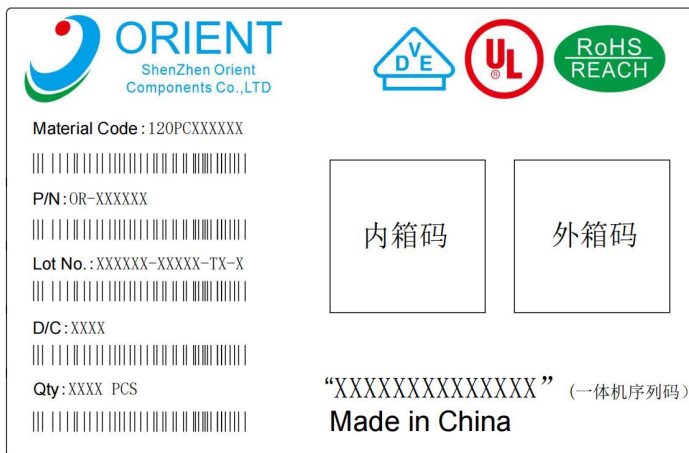
Encapsulation type	TP/TP1
amount (pcs)	3000

#### 4. Package Dimension

##### (1) package dimension

Packing Information	
Packing type	Reel type
Tape Width	12mm
Qty per Reel	3,000pcs
Small box (inner) Dimension	345*345*45mm
Large box (Outer) Dimension	480x360x360mm
Max qty per small box	6,000pcs
Max qty per large box	60,000pcs

##### (2) Packing Label Sample



**Note:**

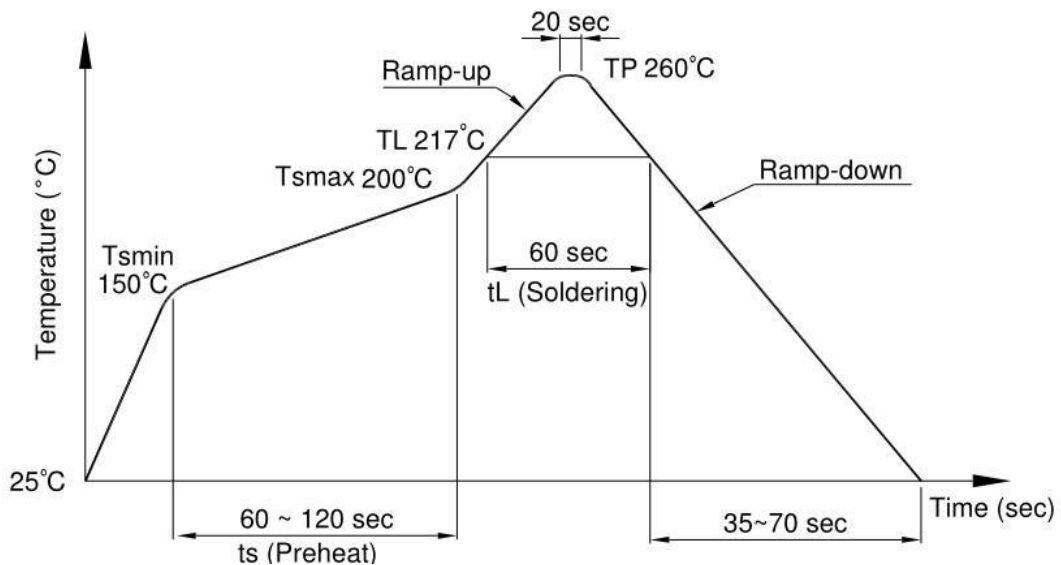
1. Material Code :Product ID.
2. P/N :Contents with "Order Information" in the specification.
3. Lot No. :Product data.
4. D/C :Product weeks.
5. Quantity :Packaging quantity.

### 11. Temperature Profile Of Soldering

(1).IR Reflow soldering (JEDEC-STD-020C compliant)

One time soldering reflow is recommended within the condition of temperature and time profile shown below. Do not solder more than three times.

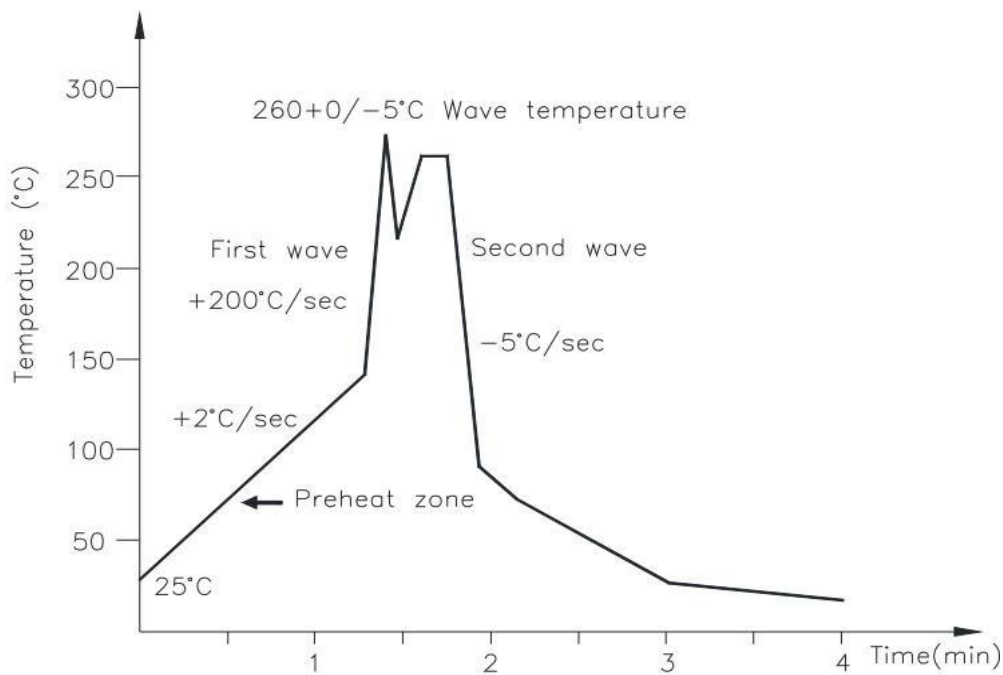
Profile item	Conditions
Preheat - Temperature Min (T Smin ) - Temperature Max (T Smax ) - Time (min to max) (ts)	150°C 200°C 90±30 sec
Soldering zone - Temperature (TL ) - Time (t L )	217°C 60 sec
Peak Temperature	260°C
Peak Temperature time	20 sec
Ramp-up rate	3°C / sec max.
Ramp-down rate from peak temperature	3~6°C / sec
Reflow times	≤3



**(3) .Wave soldering (JEDEC22A111 compliant)**

One time soldering is recommended within the condition of temperature.

Temperature	260+0/-5°C
Time	10 sec
Preheat temperature	5 to 140°C
Preheat time	30 to 80 sec



**(3).Hand soldering by soldering iron**

Allow single lead soldering in every single process. One time soldering is recommended.

Temperature	380+0/-5°C
Time	3 sec max

## 12. CHARACTERISTICS CURVES (TYPICAL PERFORMANCE)

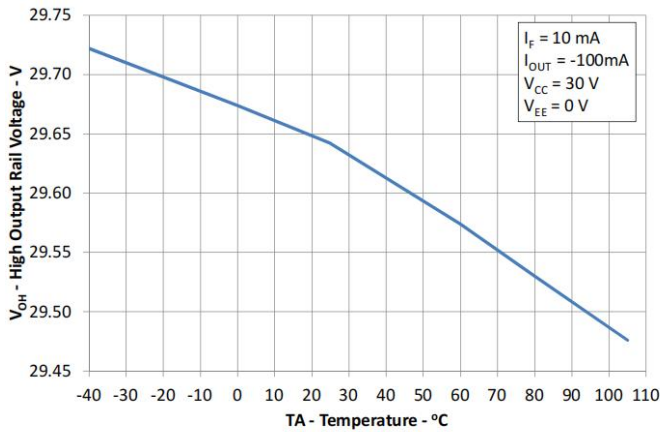


Figure 1: High output rail voltage vs. Temperature

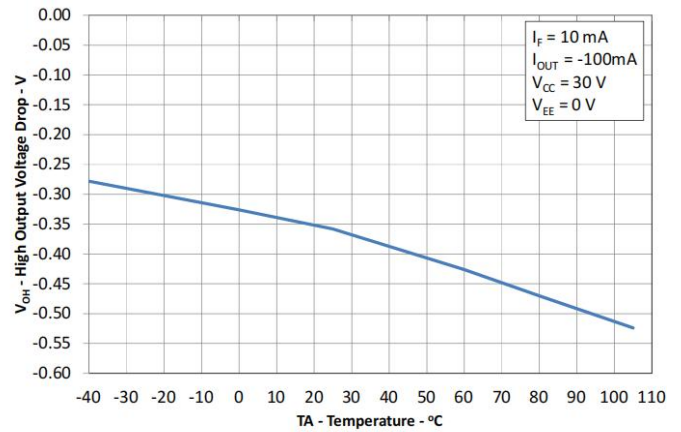


Figure 2:  $V_{OH}$  vs. Temperature

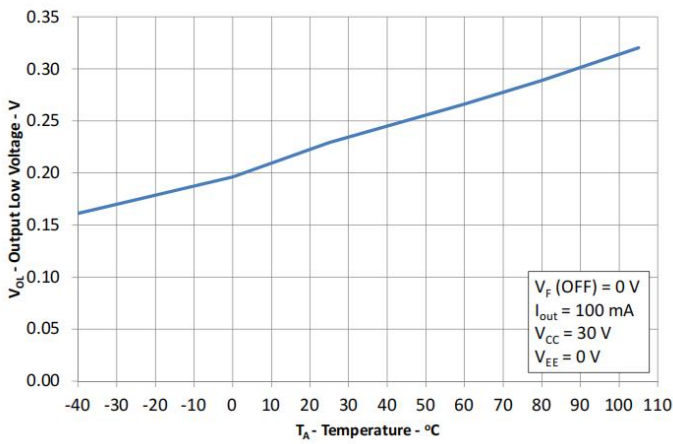


Figure 3:  $V_{OL}$  vs. Temperature

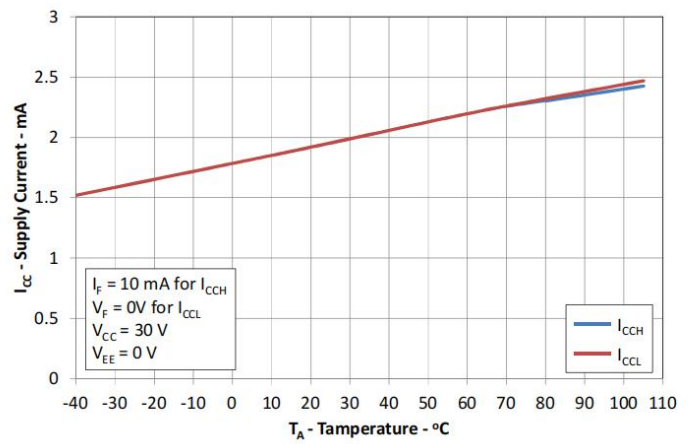


Figure 4:  $I_{CC}$  vs. Temperature

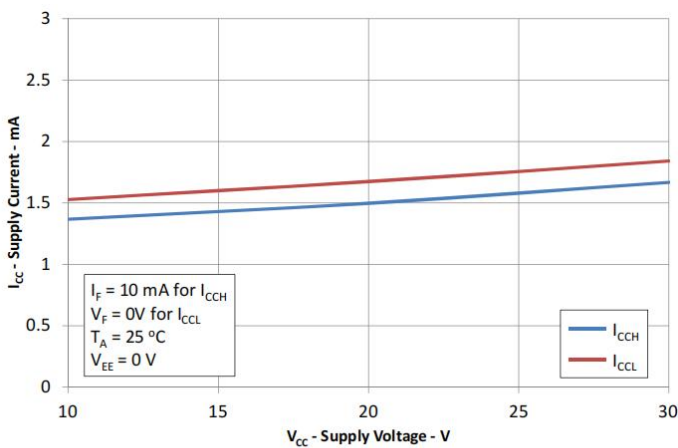


Figure 5:  $I_{CC}$  vs.  $V_{CC}$

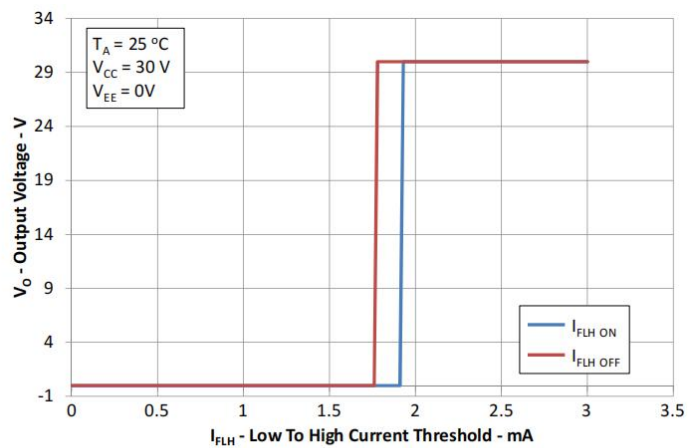


Figure 6:  $I_{FLH}$  hysteresis

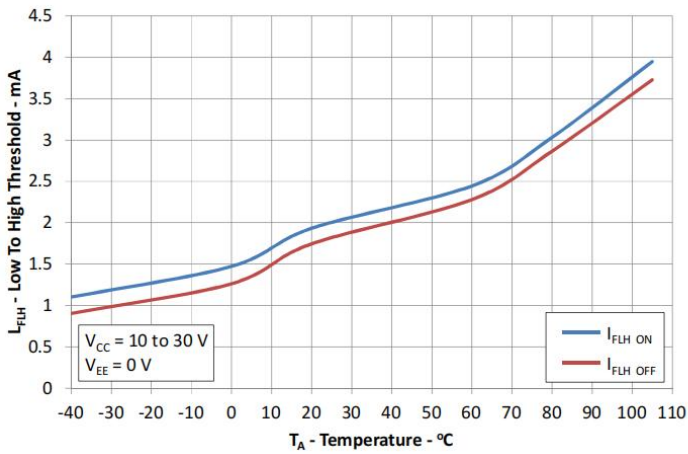


Figure 7:  $I_{FLH}$  vs. Temperature

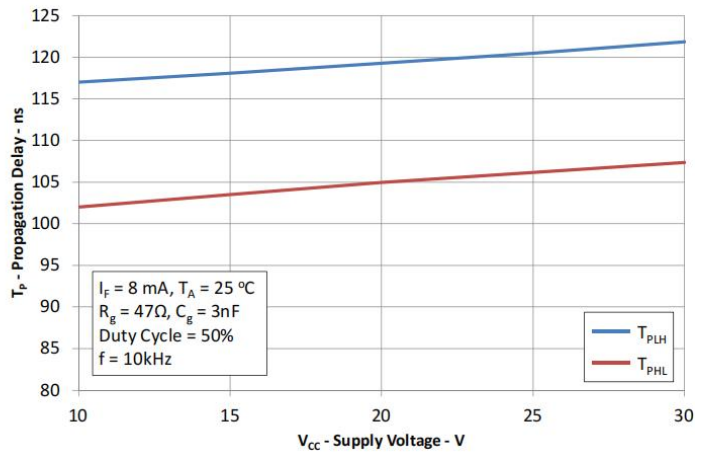


Figure 8: Propagation delays vs.  $V_{CC}$

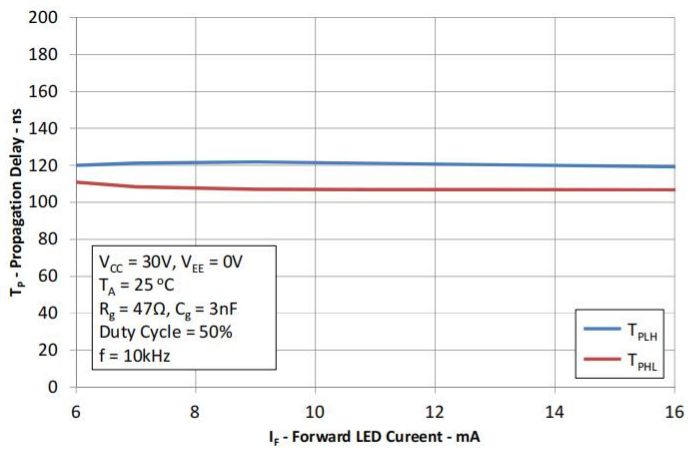


Figure 9: Propagation delays vs.  $I_F$

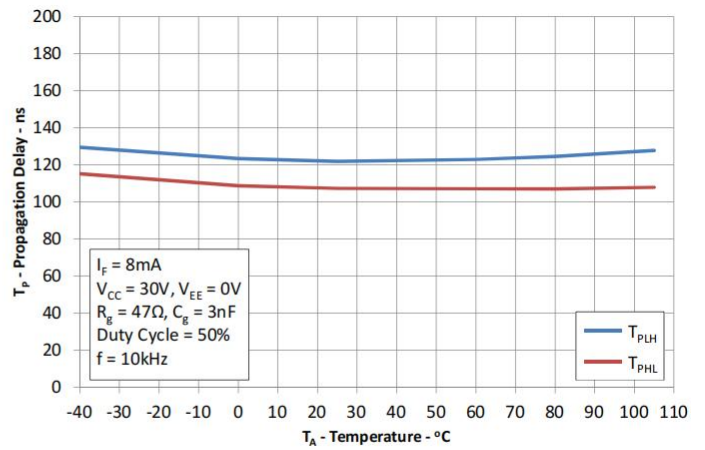


Figure 10: Propagation delays vs. Temperature

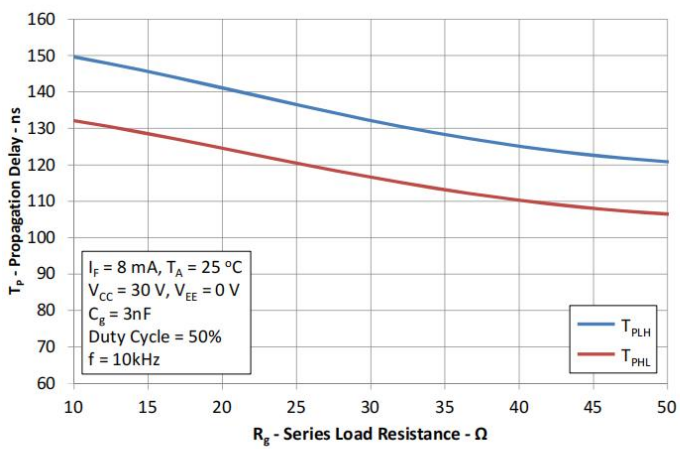


Figure 11: Propagation delays vs.  $R_g$

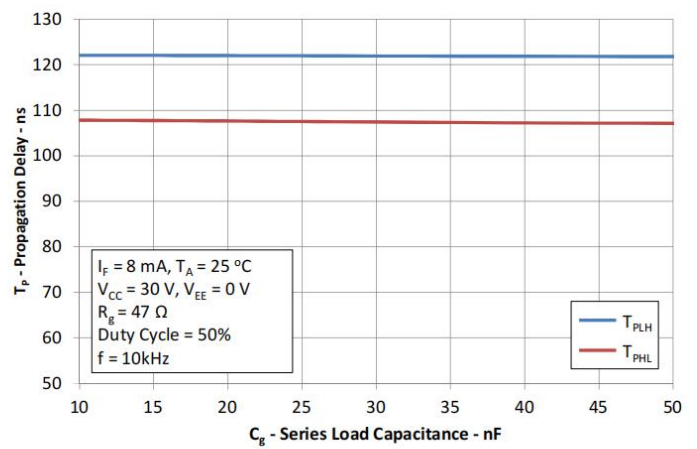


Figure 12: Propagation delays vs.  $C_g$

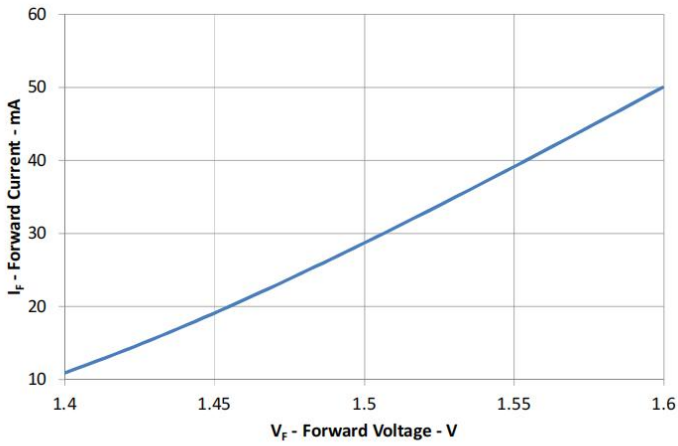


Figure 13: Input current vs. Forward voltage

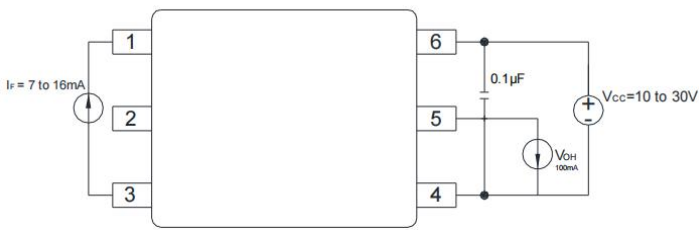


Figure 14 :  $V_{OH}$  Test Circuit

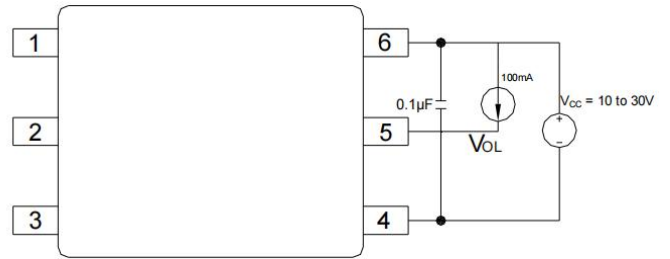


Figure 15 :  $V_{OL}$  Test Circuit

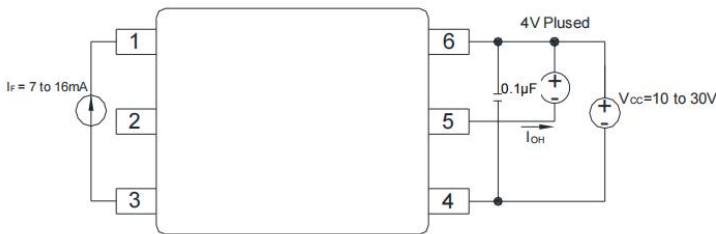


Figure 16 :  $I_{OH}$  Test Circuit

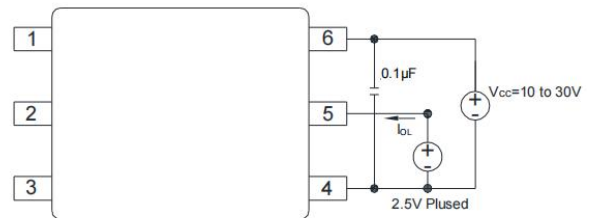


Figure 17 :  $I_{OL}$  Test Circuit

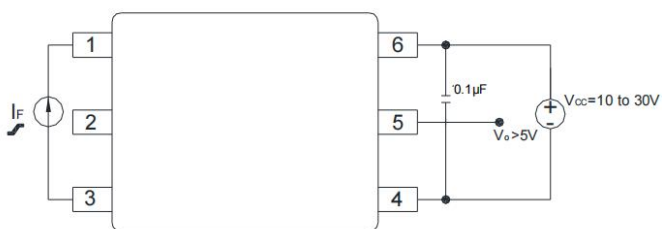


Figure 18 :  $I_{FLH}$  Test Circuit

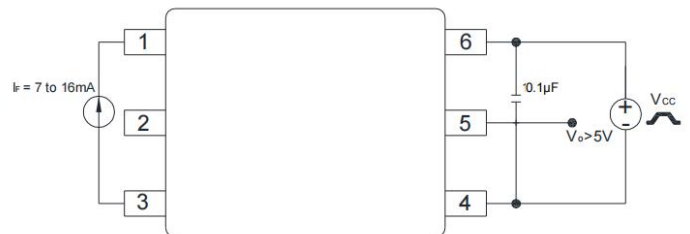


Figure 19 : UVLO Test Circuit

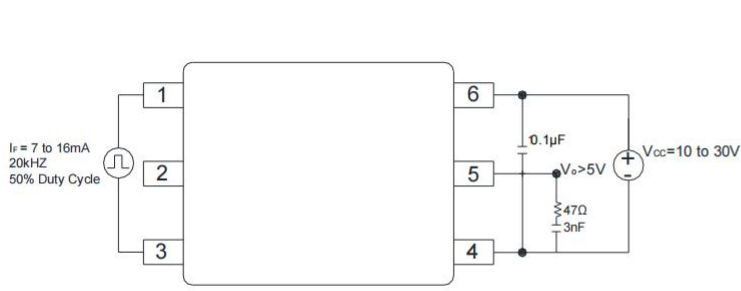


Figure 20 :  $t_r$ ,  $t_f$ ,  $t_{PLH}$  and  $t_{PHL}$  Test Circuit and Waveforms

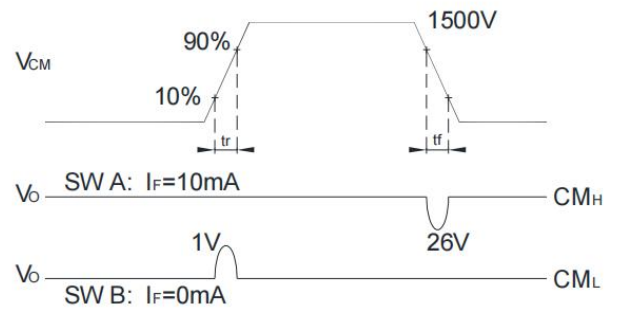
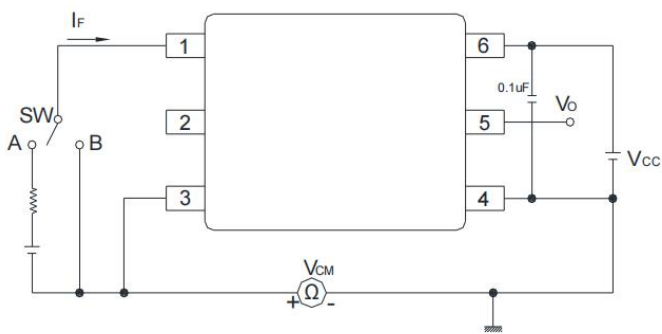


Figure 21 : CMR Test Circuit and Waveforms