ORIENT

Photo coupler

Product Data Sheet

Part Number: OR-H61L

Customer: _____

Date: _____

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1. Features

(1) Low I_{DD} power supply consumption: 2 mA max.
(2) Input current capability: 4.5 mA min.
(3) Package: 15-mm stretched SO-8.
(4) 20 kV/μs minimum common-mode rejection (CMR) at V_{CM} = 1000 V.
(5) High speed: 10 MBd min.
(6) Guaranteed AC and DC performance over temperature: –40°C to +105°C.
(7) In compliance with RoHS, REACH standards
(8) MSL Level 1

2. Description

The OR-H61L is a stretched wide optically coupled optocoupler that combines a light-emitting diode and an integrated high gain photo detector to address the low power need for isolated interface. The optocoupler consumes extremely low power, at maximum 2 mA across temperature. The LED forward current operates from 4.5 mA.

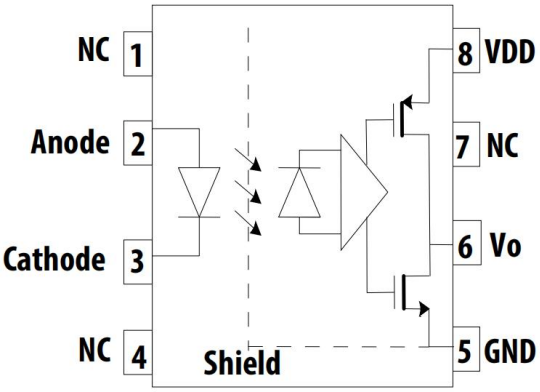
This optocoupler supports both a 3.3V and a 5V supply voltage with guaranteed AC and DC operational parameters from temperature range –40°C to +105°C. The output of the detector IC is a CMOS output. The internal Faraday shield provides a guaranteed common-mode transient immunity specification of 20 kV/μs.

The OR-H61L with 15-mm stretched SO-8 package and high voltage insulation capability is suitable for isolated communicate logic interface and control in high-voltage power systems such as 690VAC drives, renewable inverters, and medical equipment.

3. Application Range

(1) Communication Interface: RS-485, CAN bus
(2) Digital isolation for A/D, D/A conversion
(3) High-voltage power systems, e.g., 690V drives
(4) Renewable energy inverters
(5) Medical imaging and patient monitoring

4. Functional Diagram



Truth Table (Positive Logic)

LED	Output V_O
ON	L
OFF	H

A 0.1-μF bypass capacitor must be connected between pins V_{CC} and GND.

5. Absolute Maximum Ratings (Ta=25°C)

Parameter		Symbol	Ratings	Unit
INPUT	Forward Current	I_F	10	mA
	Peak Forward Input Current	$I_{F(TRAN)}$	1	A
	Reverse Voltage	V_R	5	V
	Input Power Dissipation	P_I	20	mW
OUTPUT	Supply Voltage	V_{DD}	6.5	V
	Enable Input Current	I_E	8	mA
	Output Collector Current	I_O	10	mA
	Output Collector Voltage	V_O	–0.5 ~ VDD + 0.5	V
	Output Collector Power Dissipation	P_O	22	mW
Isolation Voltage*2		V_{ISO}	7500	Vrms.
Operating Ambient Temperature		T_{Opr}	–40 to +105	°C
Storage Temperature		T_{stg}	–55 to +125	°C

6. Electrical Specifications (DC)

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input Forward Voltage	V_F	1.20	1.38	1.85	V	I_F = 7 mA
Input Reverse Breakdown Voltage	BV_R	7	—	—	V	I_R = 10 µA
Logic High Output Voltage	V_{OH}	V_{DD} – 0.1	V_{DD}	—	V	I_F = 0 mA, V_I = 0V, I_O = –20 µA
		V_{DD} – 1.0	V_{DD}	—	V	I_F = 0 mA, V_I = 0V, I_O = –3.2 mA
Logic Low Output Voltage	V_{OL}	—	0.02	0.1	V	I_F = 7 mA, V_I = 5V/3.3V, I_O = 20 µA
		—	0.2	0.4	V	I_F = 7 mA, V_I = 5V/3.3V, I_O = 3.2 mA
Input Threshold Current	I_{TH}	—	0.7	3.8	mA	—
Logic Low Output Supply Current	I_{DDL}	—	1	2	mA	—
Logic High Output Supply Current	I_{DDH}	—	1	2	mA	—
Input Capacitance	C_{IN}	—	20	—	pF	f = 1 MHz, V_F = 0V
Input Diode Temperature Coefficient	$\Delta V_F/\Delta T_A$	—	–1.5	—	mV/°C	I_F = 7 mA

Over recommended temperature (TA = –40°C to +105°C), supply voltage (2.7V ≤ VDD ≤ 5.5V). All typical specifications are at VDD = 5V, TA = 25°C.

7. Switching Specifications (AC)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Propagation Delay Time to Logic Low Output*1	t_{PHL}	—	40	100	ns	I_F = 7 mA, V_I = 3.3V/5V, C_L= 15 pF, CMOS Signal Levels.
Propagation Delay Time to Logic High Output*1	t_{PLH}	—	40	100	ns	
Pulse Width	t_{PW}	100	—	—	ns	
Pulse Width Distortiont*2	PWD	—	5	40	ns	
Propagation Delay Skewt*3	t_{PSK}	—	—	40	ns	
Output Rise Time (10% to 90%)	t_R	—	10	—	ns	
Output Fall Time (90% to 10%)	t_F	—	10	—	ns	
Static Common-Mode Transient Immunity at Logic High Outputt*4	$\lvert CM_H \rvert$	20	35	—	kV/μs	V_{CM} = 1000V, T_A = 25°C, I_F = 0 mA, V_I = 0V, C_L= 15 pF, CMOS Signal Levels
Static Common-Mode Transient Immunity at Logic Low Outputt*5	$\lvert CM_L \rvert$	20	35	—	kV/μs	V_{CM} = 1000 V, T_A = 25°C, I_F = 7 mA, V_I = 5V/3.3V, C_L= 15 pF, CMOS Signal Levels
Dynamic Common-Mode Transient Immunityt*6	CMRD	—	35	—	kV/μs	V_{CM} = 1000V, T_A = 25°C, I_F = 7 mA, V_I = 5V/3.3V, 10-MBd data rate, the absolute increase of PWD <10 ns

1. t_{PHL} propagation delay is measured from the 50% (V_{in} or I_F) on the rising edge of the input pulse to the 50% V_{DD} of the falling edge of the V_O signal. t_{PLH} propagation delay is measured from the 50% (V_{in} or I_F) on the falling edge of the input pulse to the 50% level of the rising edge of the V_O signal.
2. PWD is defined as $|t_{PHL} - t_{PLH}|$.
3. t_{PSK} is equal to the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is seen between units at any given temperature within the recommended operating conditions.
4. CM_H is the maximum tolerable rate of rise of the common-mode voltage to assure that the output remains in a high logic state.
5. CM_L is the maximum tolerable rate of fall of the common-mode voltage to assure that the output remains in a low logic state.
6. CMD is the maximum tolerable rate of the common-mode voltage during data transmission to assure that the absolute increase of the PWD is less than 10 ns.

8. Order Information

Part Number

OR-H61L-Z

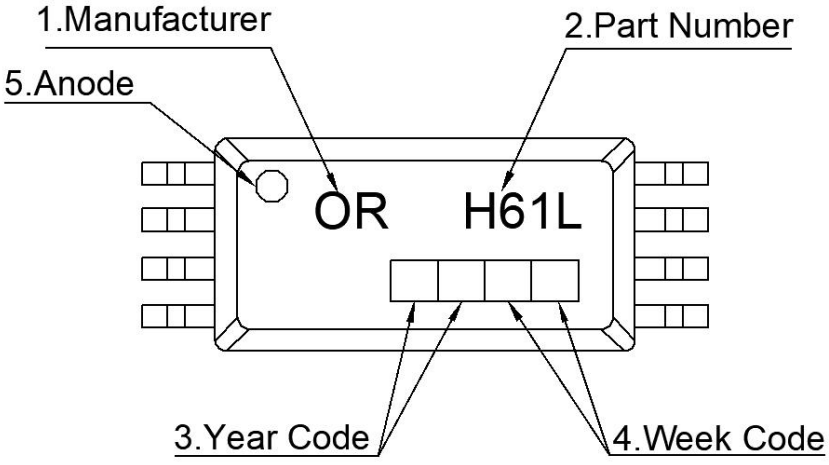
Note

H61L = Part Number.

Y = Tape and reel option (TA,TA1 or none).

Option	Description	Packing quantity
S(TA)	Surface mount lead form (low profile) + TA tape & reel option	1000 units per reel
S(TA1)	Surface mount lead form (low profile) + TA1 tape & reel option	1000 units per reel

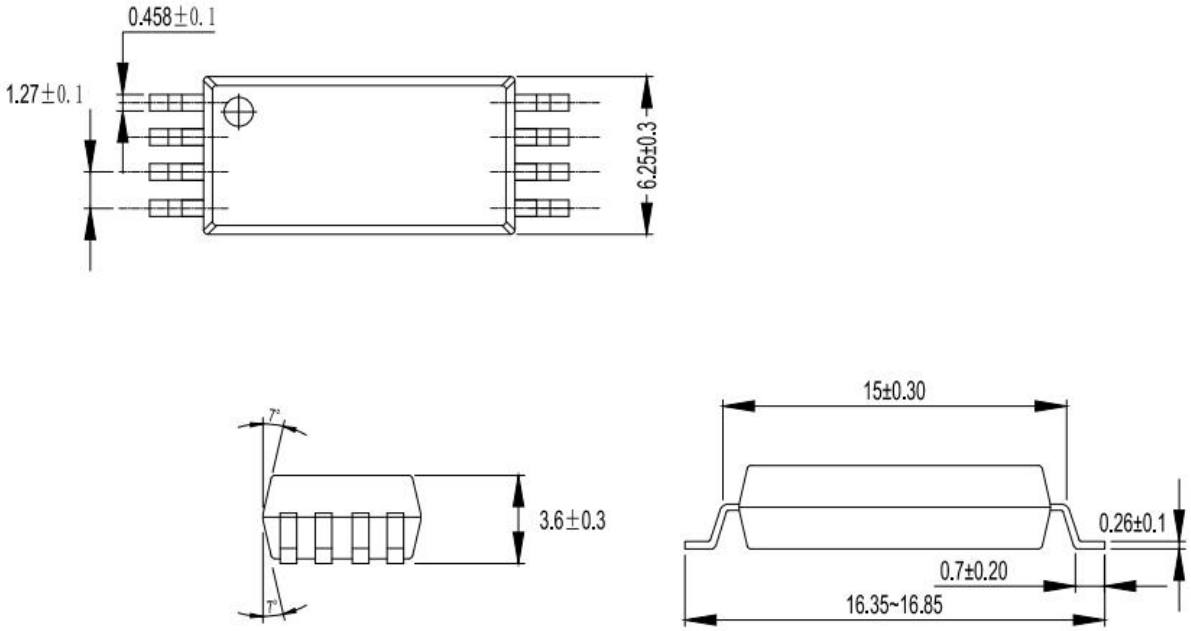
9. Naming Rule



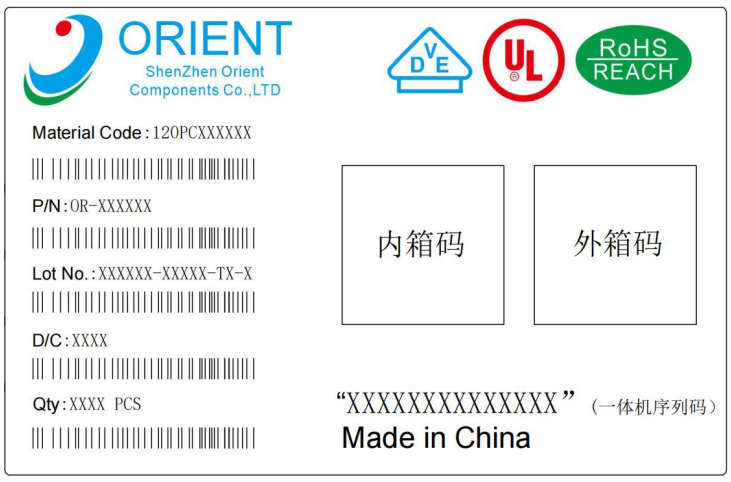
1. Manufacturer : ORIENT.
2. Part Number : H61L.
3. Year Code □□ : '21' means '2021' and so on.
4. Week Code □□: 01 means the first week, 02 means the second week and so on.
5. Anode.

10. Package Dimension

OR-H61L



11. Package Dimension



Note:

1. Material Code :Product ID.
2. P/N :Contents with "Order Information" in the specification.
3. Lot No. :Product data.
4. D/C :Product weeks.
5. Quantity :Packaging quantity.

12. Reliability Test

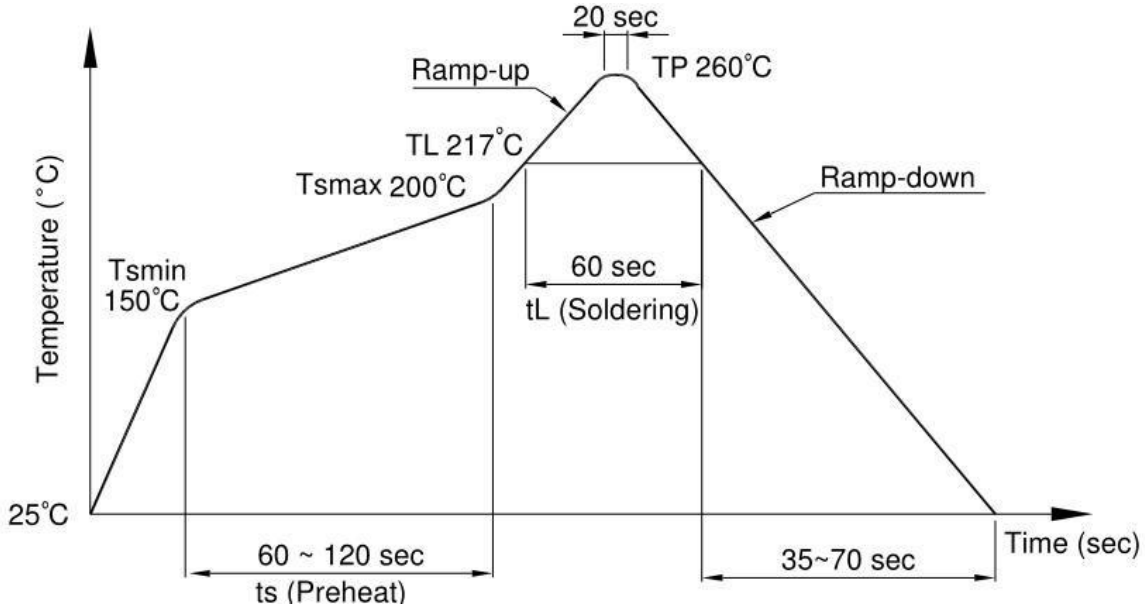
NO.	ITEMS	Reliability Testing				
		QTY. (Pcs)	Condition	Process	Device	Standard
1	RSH 耐焊接热	22	260±5°C	5s/3 次	锡炉	JESD22-A106
2	HTSL 高温存储	77	125°C	168 hrs 500 hrs 1000 hrs	高温烤箱测试仪	JESD22-A103
3	LTSL 低温存储	77	-40°C	168 hrs 500 hrs 1000 hrs	低温箱测试仪	JESD22-A119
4	TC 温度循环	77	H:125°C 15min ∫5min L:-55°C 15min	300 cycle	冷热冲击机	JESD22-A104
5	TS 温度冲击	77	H:100°C 5min ∫15s L:-40°C 5min	300 cycle	冷热冲击机	JESD22-A106
6	HTOL 高温操作	77	100°C IF=10mA Vcc=5V	168 hrs 500 hrs 1000 hrs	高温烤箱测试仪、老化电路板	JESD22-A108
7	ESD-HBM 人体模式	22	≥8KV 1Cycle	1次	ESD静电测试仪	JESD22-A114
8	SD 可焊性	22	Pb-free 245±5°C	5s/1次	锡炉	JESD22-B102
9	HTHB 温湿寿命试验	77	85°C,85%RH IF=10mA,Vcc=5V	168 hrs 500 hrs 1000 hrs	恒温恒湿机，测试仪	JESD22-A101
10	Autoclave 压力锅	77	Ta=121 °C,100%RH,2atm	96hrs	压力锅	JESD22-A102

13. Temperature Profile Of Soldering

(1).IR Reflow soldering (JEDEC-STD-020C compliant)

One time soldering reflow is recommended within the condition of temperature and time profile shown below. Do not solder more than three times.

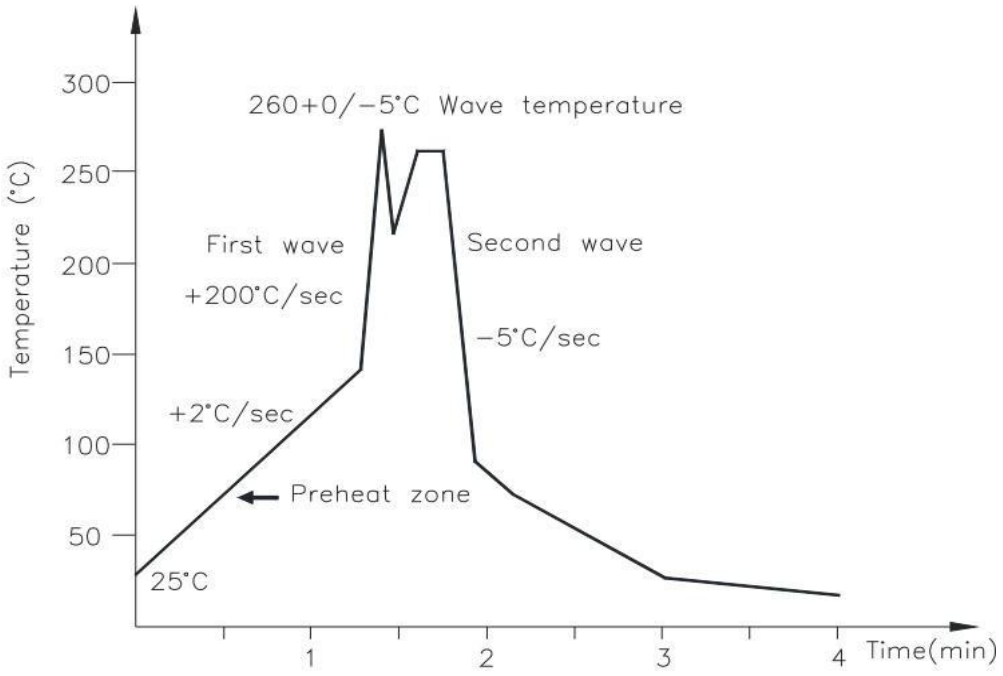
Profile item	Conditions
Preheat - Temperature Min (T Smin) - Temperature Max (T Smax) - Time (min to max) (ts)	 150˚C 200˚C 90±30 sec
Soldering zone - Temperature (TL) - Time (t L)	 217˚C 60 sec
Peak Temperature	260˚C
Peak Temperature time	20 sec
Ramp-up rate	3˚C / sec max.
Ramp-down rate from peak temperature	3~6˚C / sec
Reflow times	≤3



(3) .Wave soldering (JEDEC22A111 compliant)

One time soldering is recommended within the condition of temperature.

Temperature Time	260+0/-5˚C 10 sec
Preheat temperature Preheat time	5 to 140˚C 30 to 80 sec



(3).Hand soldering by soldering iron

Allow single lead soldering in every single process. One time soldering is recommended.

Temperature Time	380+0/-5˚C 3 sec max

14. CHARACTERISTICS CURVES (TYPICAL PERFORMANCE)

Figure 1 Typical Input Diode Forward Characteristic

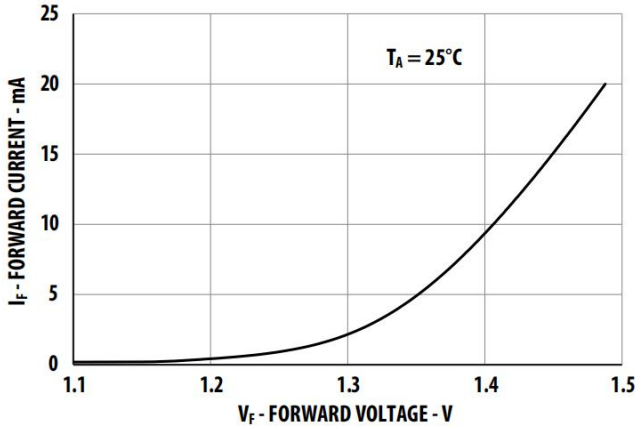


Figure 2 Typical V_F Versus Temperature

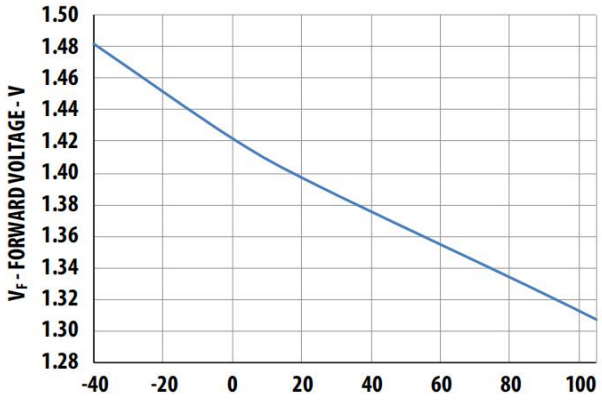


Figure 3 Typical Input Threshold Current I_{TH} Versus Temperature

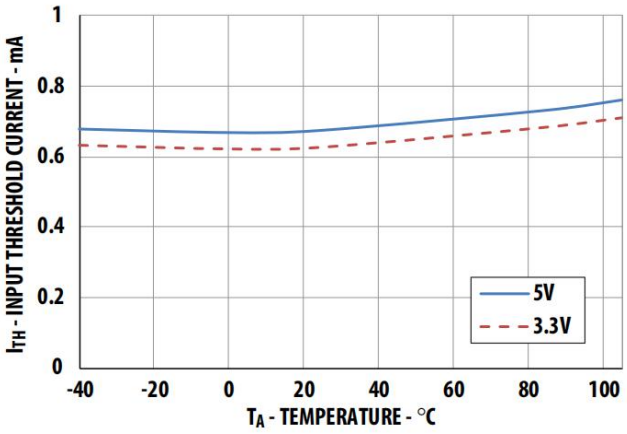


Figure 4 Typical Logic Low Output Supply Current I_{DDL} Versus Temperature

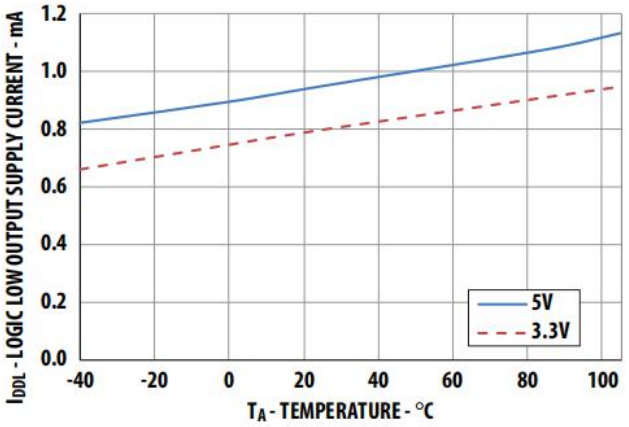


Figure 5 Typical Logic High Output Supply Current I_{DDH} Versus Temperature

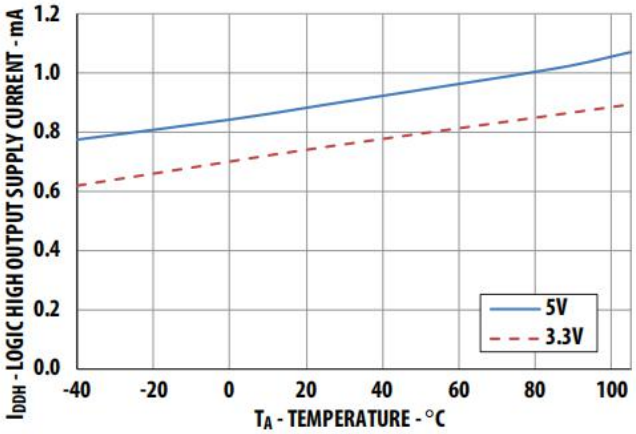


Figure 6 Typical Switching Speed Versus Pulse Input Current at 5V Supply Voltage

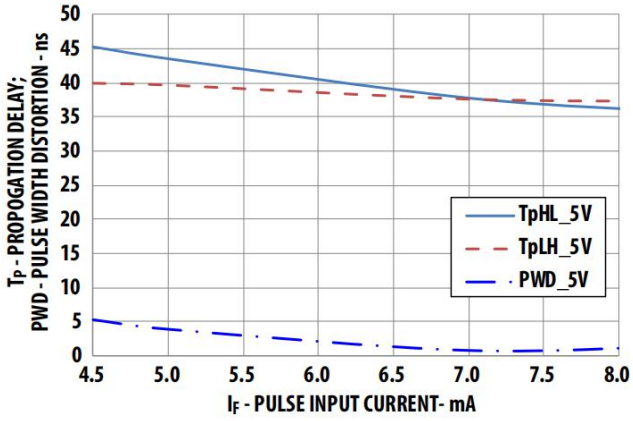


Figure 7 Typical Switching Speed Versus Pulse Input Current at 3.3V Supply Voltage

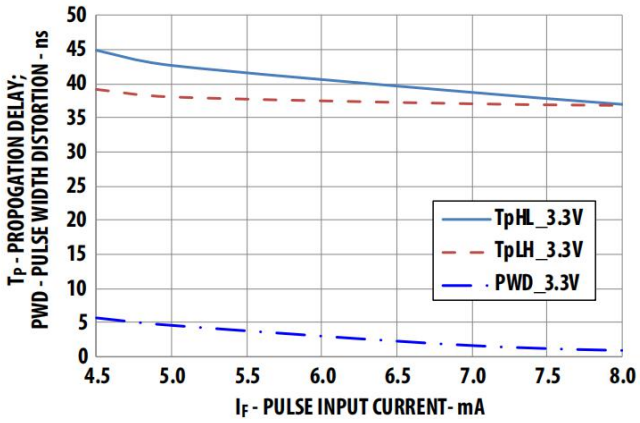


Figure 8 Typical Switching Speed Versus Temperature at 5V Supply Voltage

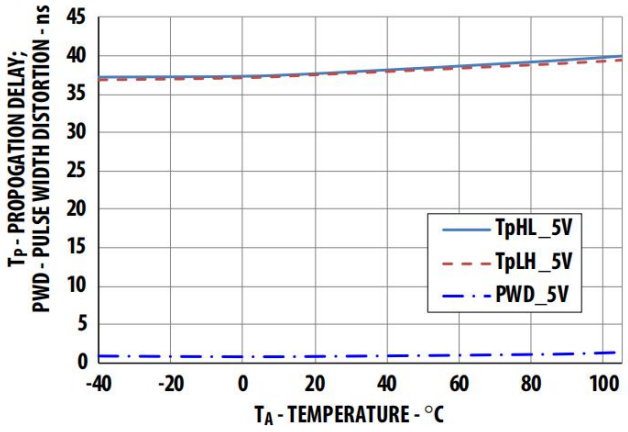


Figure 9 Typical Switching Speed Versus Temperature at 3.3V Supply Voltage

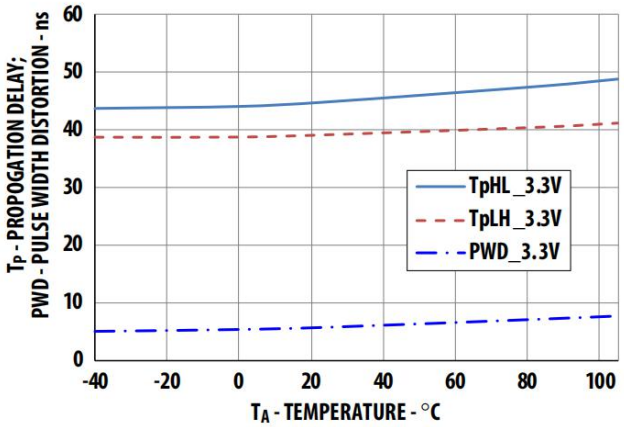


Figure 10 Recommended Printed Circuit Board Layout

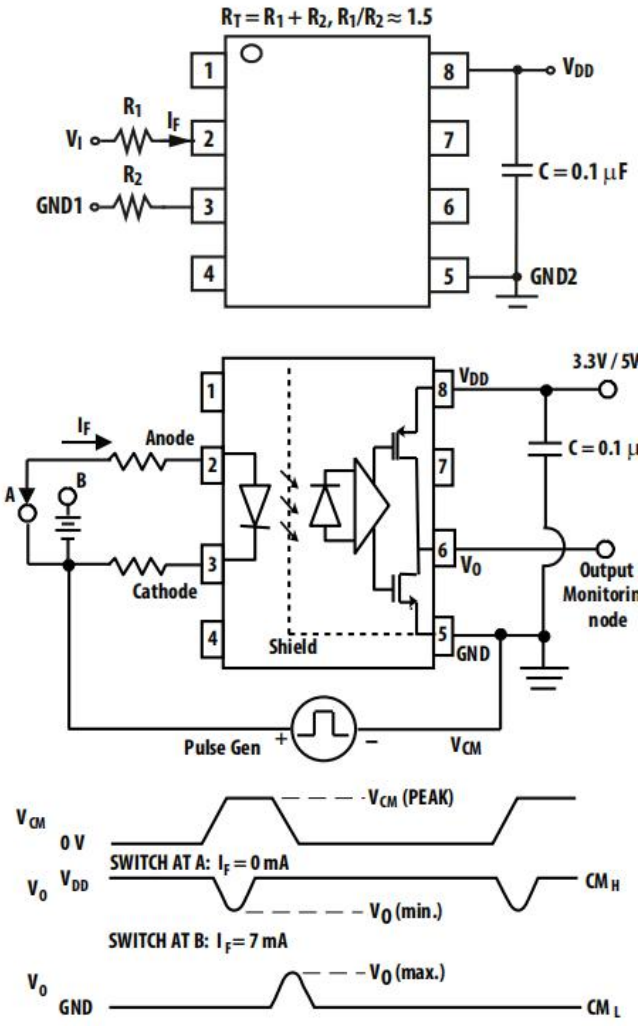


Figure 11 Propagation Delay Skew Waveform

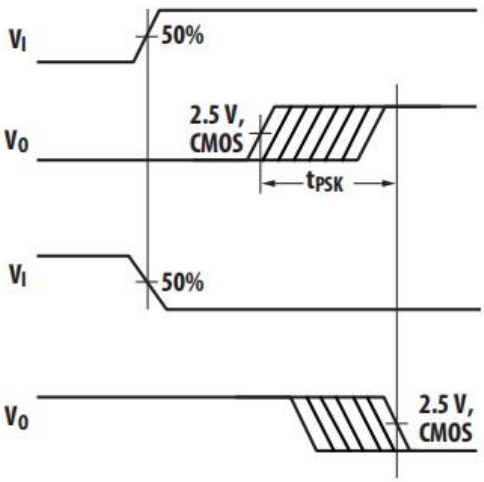


Figure 12 Parallel Data Transmission Example

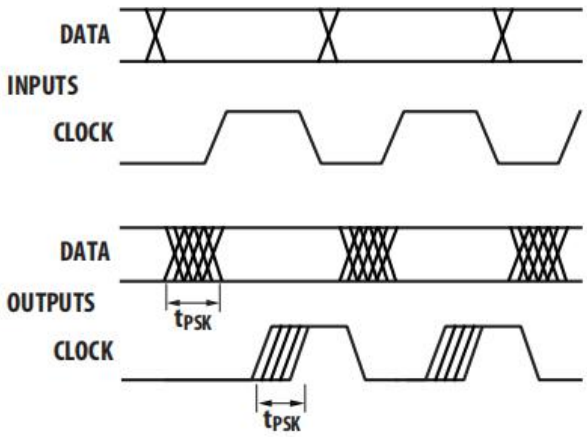


Figure 13 Recommended Drive Circuit for High-CMR

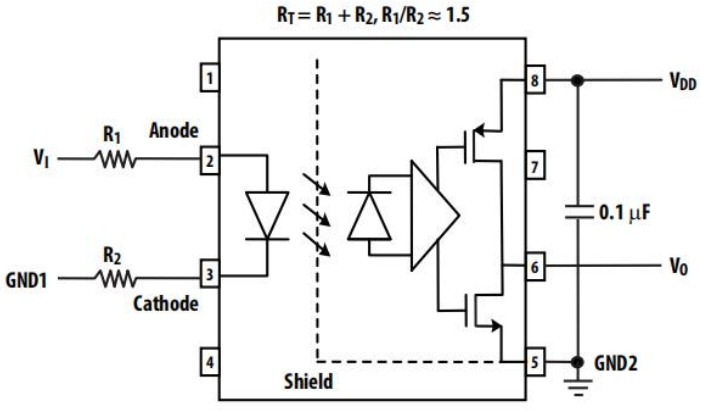


Figure 14 AC Equivalent of OR-H61L